

ABSTRACT OF THE INVENTION

A method for testing integrated circuits is provided. The method includes providing an excitation voltage to a device, such as a MOSFET. A power supply voltage is also provided to the device, such as a drain to source voltage or VCC. The quiescent power supply current of the device is then measured, such as the IDDQ of the MOSFET. The power supply voltage to the device is then varied, and it is determined whether a change in the IDDQ of the device exceeds a predetermined allowable change.